CGHV14800F1

DC-1.4 GHz, 800 W GaN Transistor

Description

The CGHV14800F1 is an 800W packaged, partially-matched transistor utilizing the high performance, 0.4um GaN on SiC production process. The CGHV14800F1 operates up to 1.4 GHz and supports both defense and commercial-related avionics and radar applications. The CGHV14800F1 typically achieves 800 W of saturated output power with 14 dB of large signal gain and 65% drain efficiency via a 1.2-1.4 GHz reference design.

Packaged in a thermally-enhanced, flange package, the CGHV14800F1 provides superior performance under long pulse operation allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Figure 1. CGHV14800F1

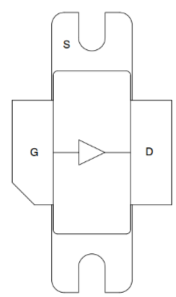


Figure 2. Functional Block Diagram

Features

- Psat: 800 W
- DE: 65 %
- LSG: 14 dB
- S21: 18 dB
- S11: -12 dB
- S22: -5 dB
- Long pulse operation

Note: Features are typical performance via a 1.2-1.4 GHz reference design under 25C, pulsed operation (CGHV14800F1-AMP). Please reference performance charts for additional information.

Applications

- Avionics - TACAN, DME, IFF
- L-band Radar
- General purpose amplification

RoHS compliant

Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain Voltage	V_d	V	50	
Gate Voltage	V_g	V	-10 to +2	
Drain Current	I_d	A	24	
Gate Current	I_g	mA	133	
Input Power	P_{in}	dBm	47	
Dissipated Power	P_{diss}	W	545	85 °C, 2ms/20%
Storage Temperature	T_{stg}	°C	-65, +150	
Mounting Temperature	T_J	°C	260	30 seconds
Junction Temperature	T_J	°C	225	MTTF > 1E6
Output Mismatch Stress	VSWR	Ψ	5:1	
Pulse Width/Duty Cycle		us/%	2000/20	85C

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	50	Pulsed only
Gate Voltage	Vg	V	-2.95	
Drain Current	Idq	mA	800	
Input Power	Pin	dBm	45	
Case Temperature	Tcase	°C	-40 to 85	

RF Specifications (CGHV14800F1-AMP)

Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, T_{base}=25 °C

Parameter	Units	Min	Typical	Max	Conditions
Frequency	GHz	1.2		1.4	
Output Power	dBm		59		Pin = 45 dBm
Drain Efficiency	%		65		Pin = 45 dBm
LSG	dB		14		Pin = 45 dBm
Small-Signal Gain (S21)	dB		18		
Input Return Loss (S11)	dB		-12		
Output Return Loss (S22)	dB		-5		

Note: Final testing and screening for all transistor sales is performed using the CGHV14800F1-AMP at 1.2-1.4 GHz.

Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency =1.4 GHz

Figure 3: Pout v. Frequency v. Temperature

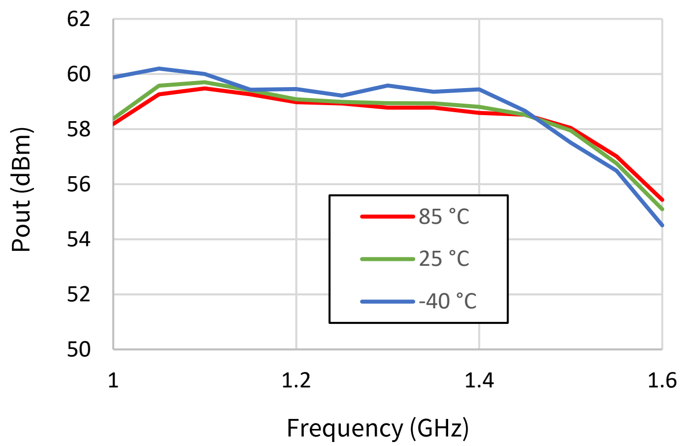


Figure 4: DE v. Frequency v. Temperature

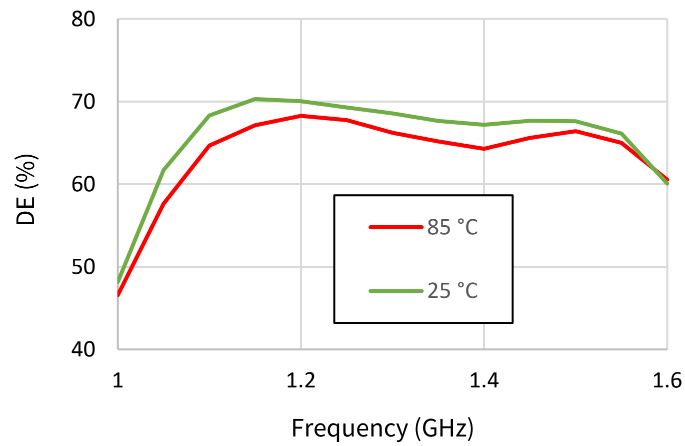


Figure 5: Id v. Frequency v. Temperature

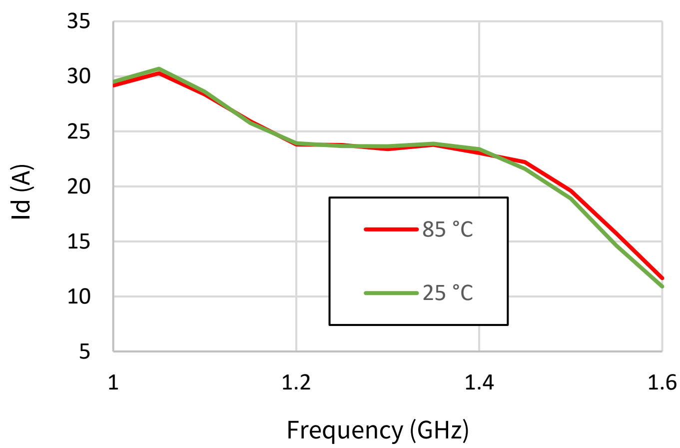


Figure 6: Ig v. Frequency v. Temperature

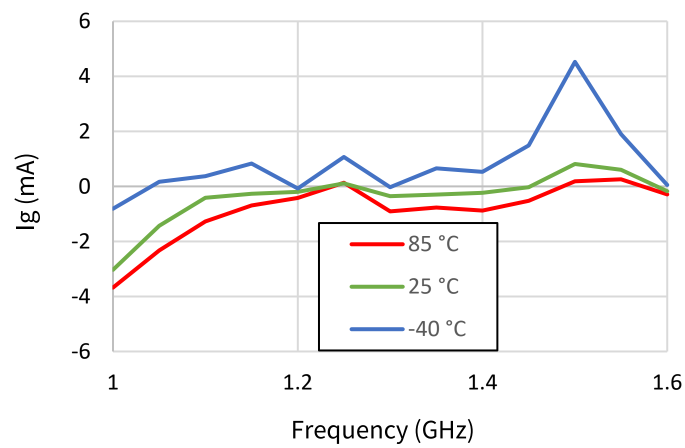
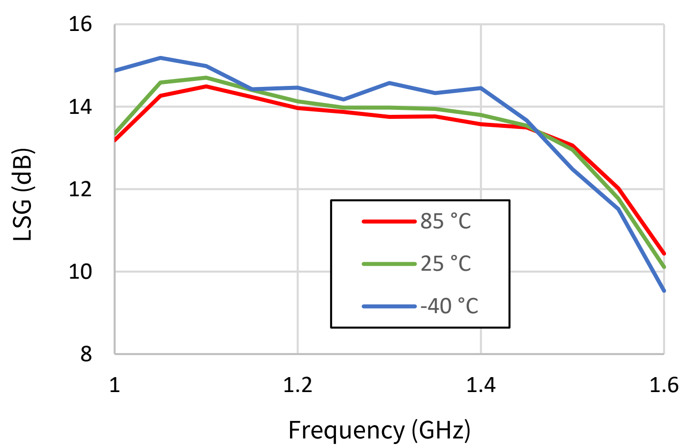


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency =1.4 GHz

Figure 8: Pout v. Frequency v. Vd

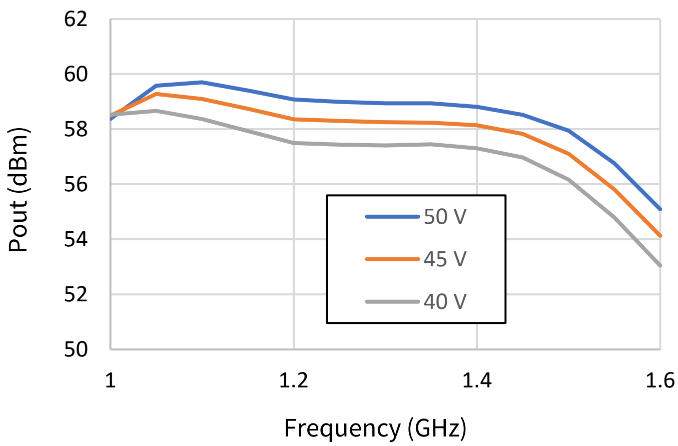


Figure 9: DE v. Frequency v. Vd

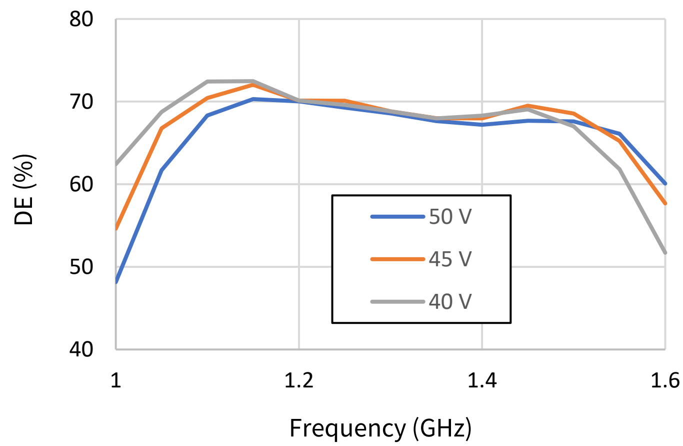


Figure 10: Id v. Frequency v. Vd

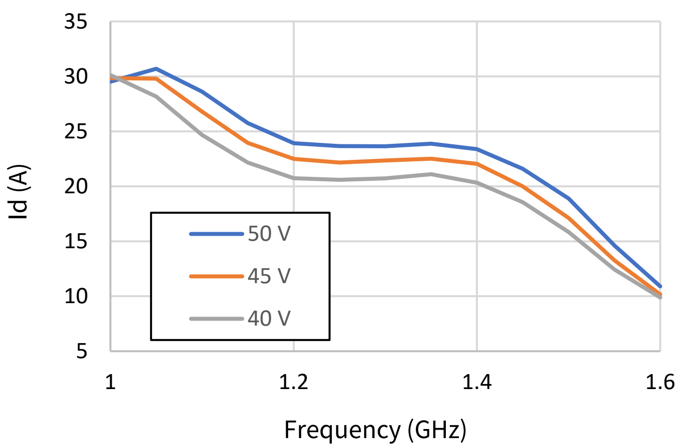


Figure 11: Ig v. Frequency v. Vd

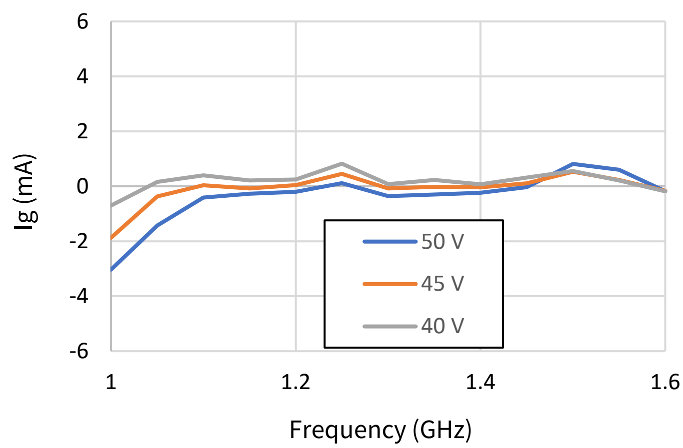
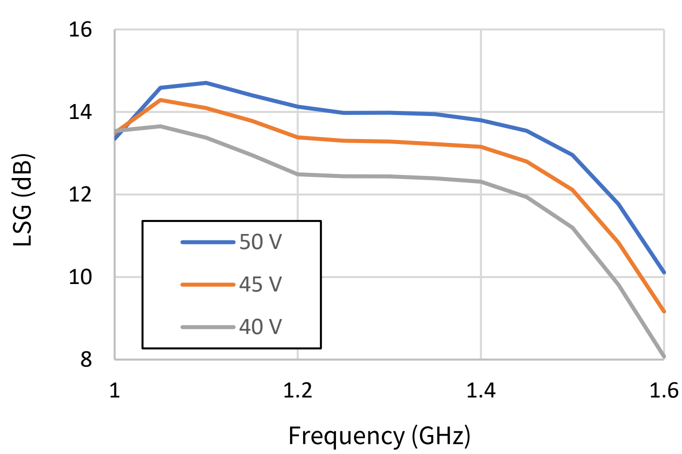


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency =1.4 GHz

Figure 13: Pout v. Frequency v. Idq

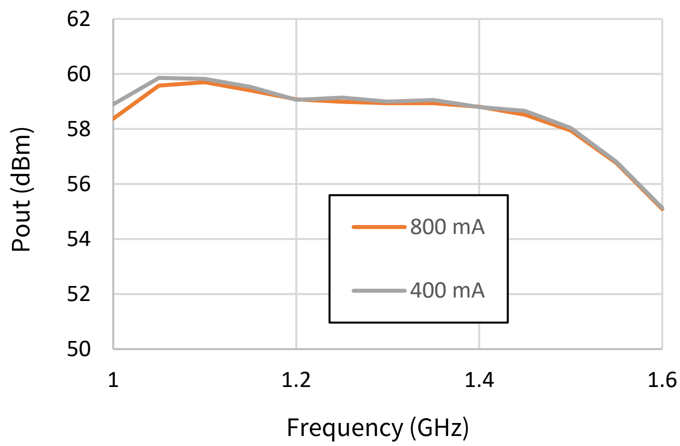


Figure 14: DE v. Frequency v. Idq

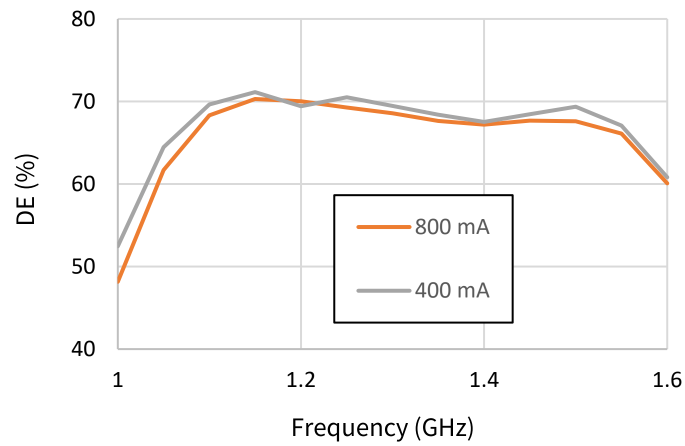


Figure 15: Id v. Frequency v. Idq

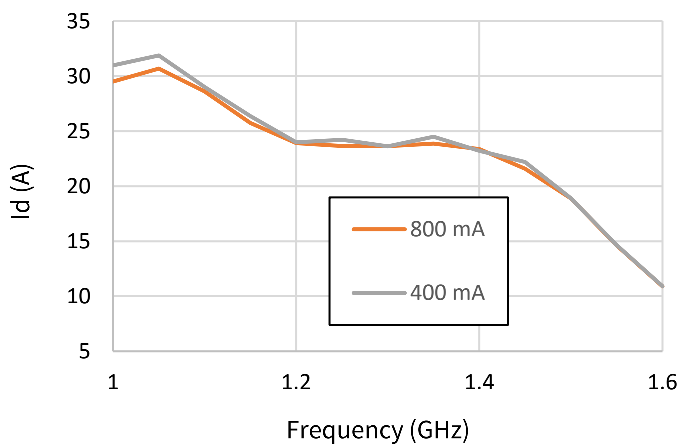


Figure 16: Ig v. Frequency v. Idq

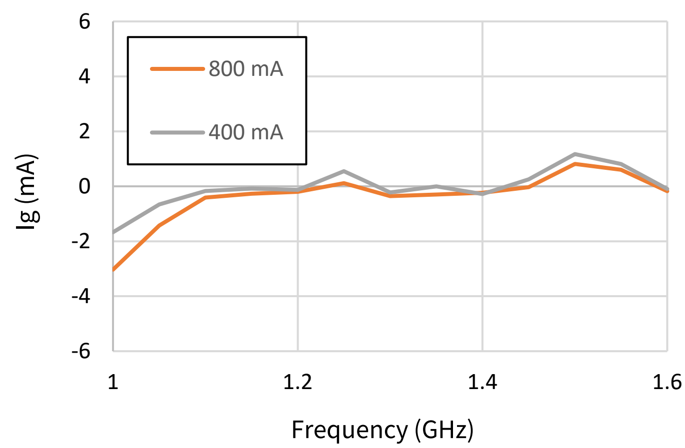
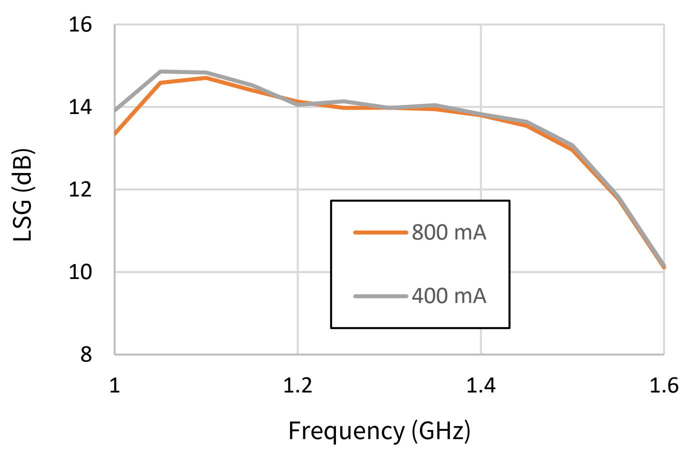


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency =1.4 GHz

Figure 18: Pout v. Pin v. Frequency

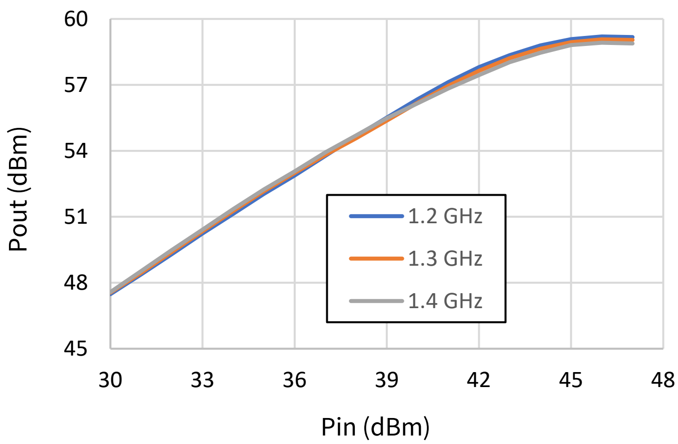


Figure 19: DE v. Pin v. Frequency

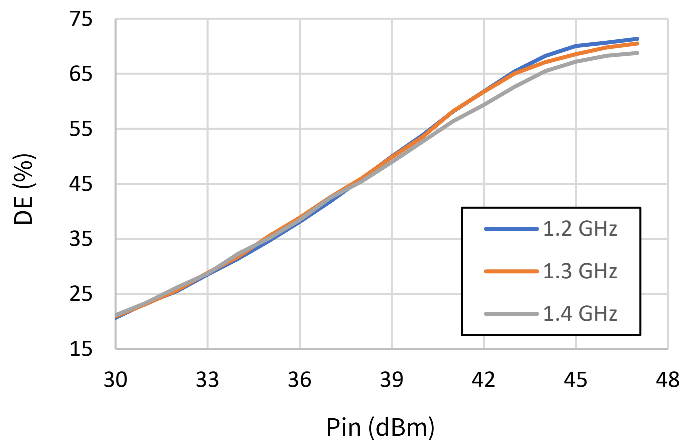


Figure 20: Id v. Pin v. Frequency

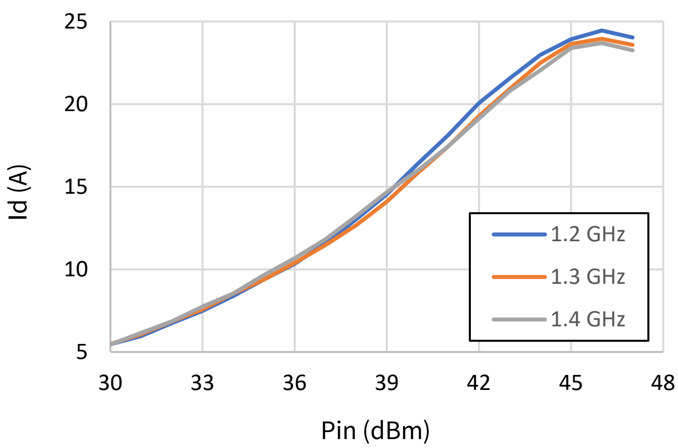


Figure 21: Ig v. Pin v. Frequency

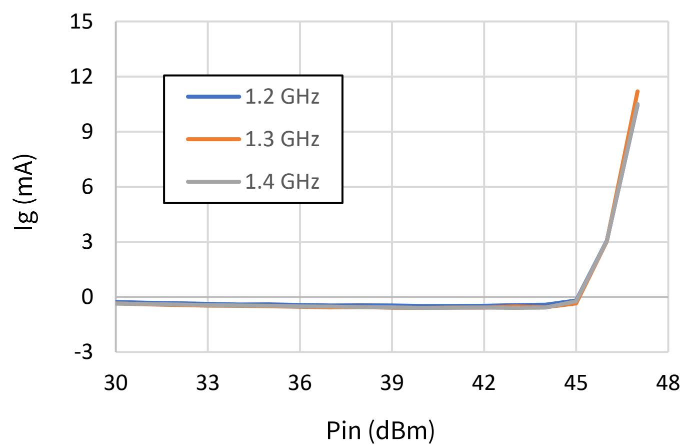
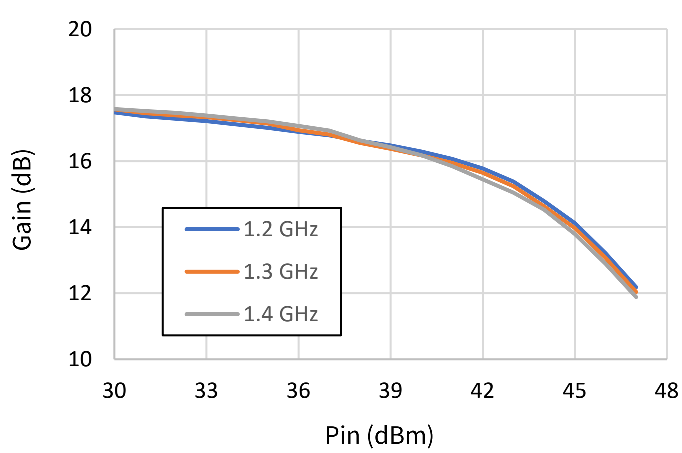


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency =1.4 GHz

Figure 23: Pout v. Pin v. Temperature

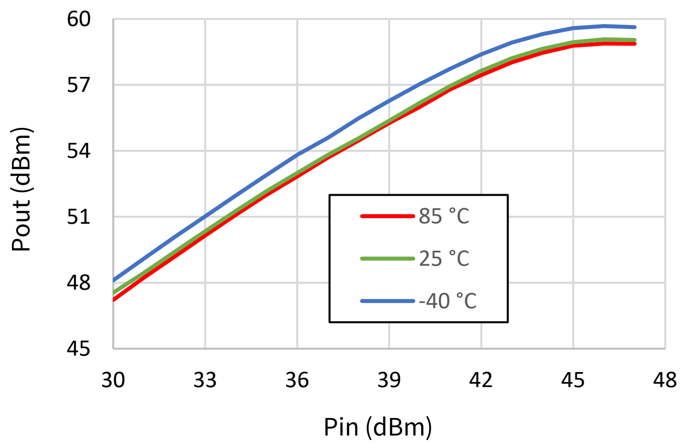


Figure 24: DE v. Pin v. Temperature

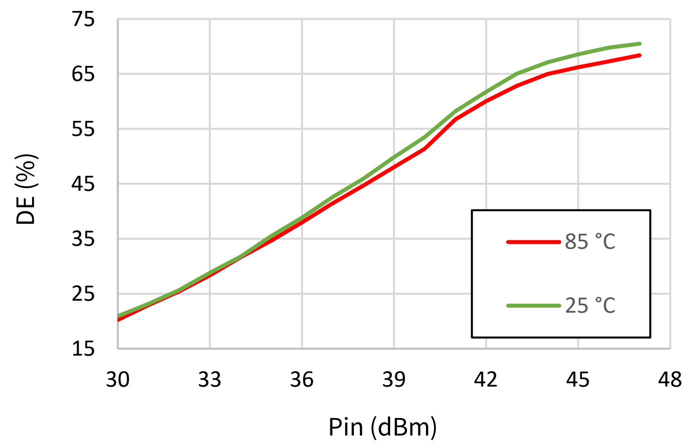


Figure 25: Id v. Pin v. Temperature

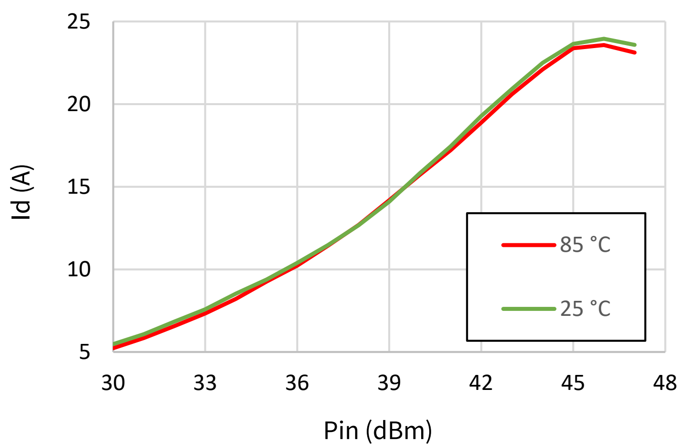


Figure 26: Ig v. Pin v. Temperature

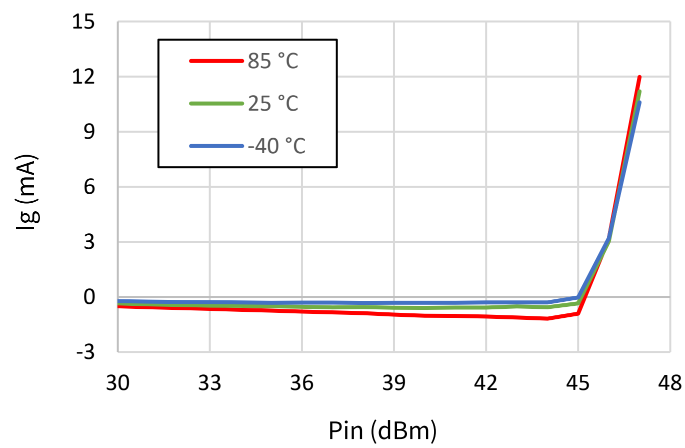
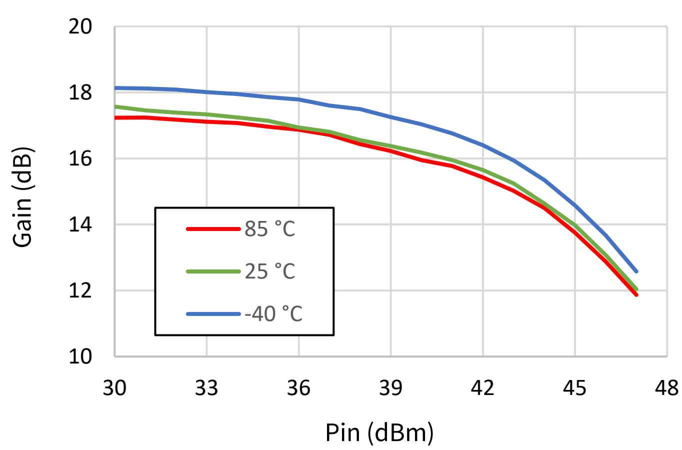


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency =1.4 GHz

Figure 28: Pout v. Pin v. Vd

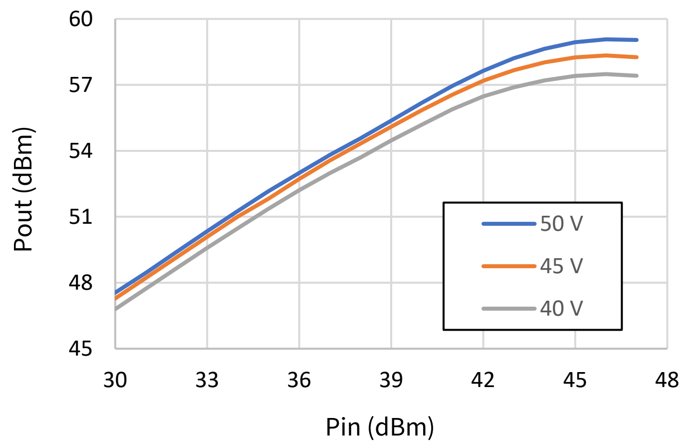


Figure 29: DE v. Pin v. Vd

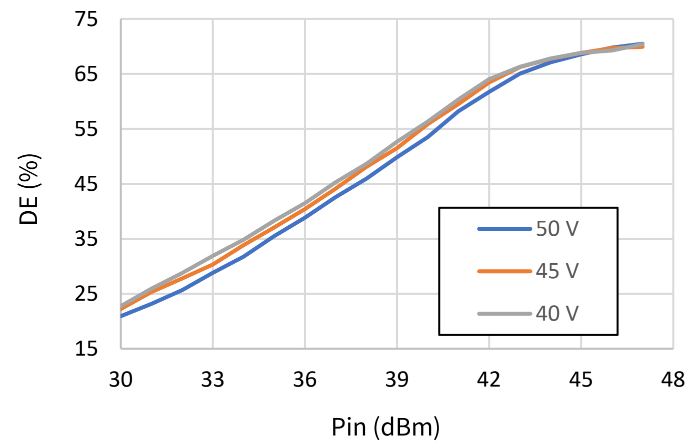


Figure 30: Id v. Pin v. Vd

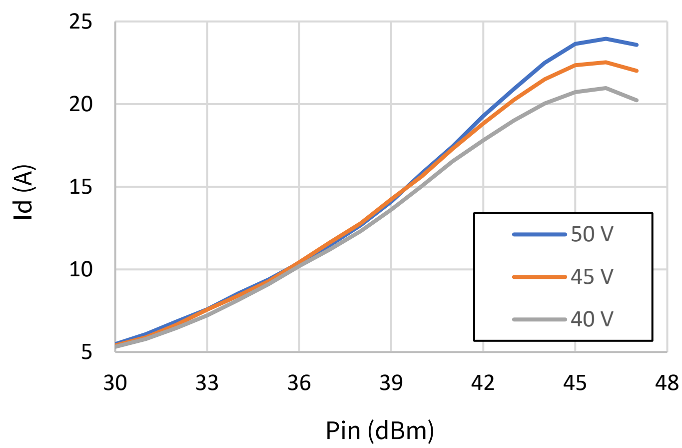


Figure 31: Ig v. Pin v. Vd

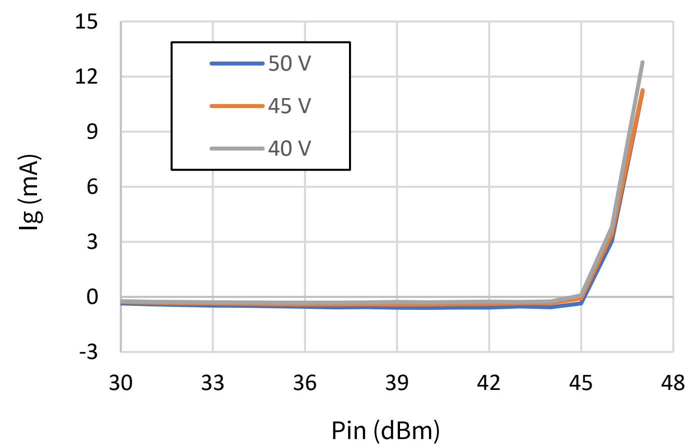
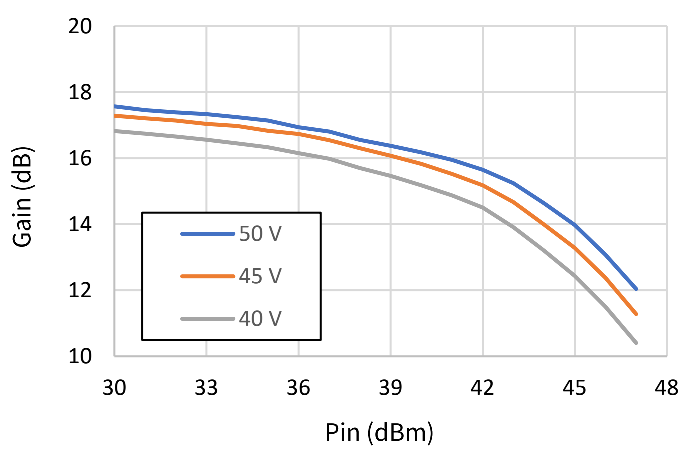


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW=2ms, DC=20%, Pin = 45dBm, T_{base}=25 °C, Frequency =1.4 GHz

Figure 33: Pout v. Pin v. Idq

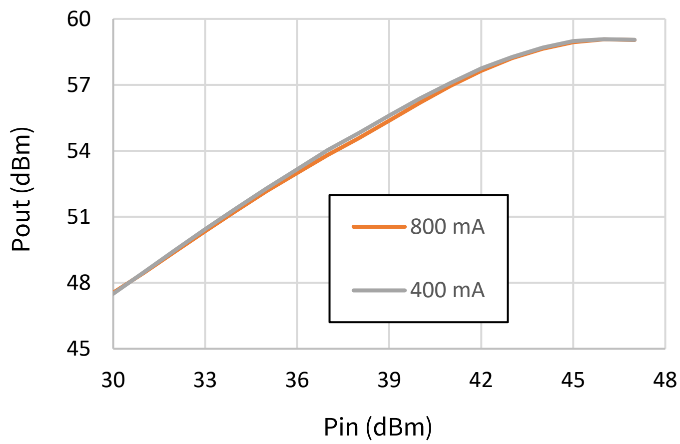


Figure 34: DE v. Pin v. Idq

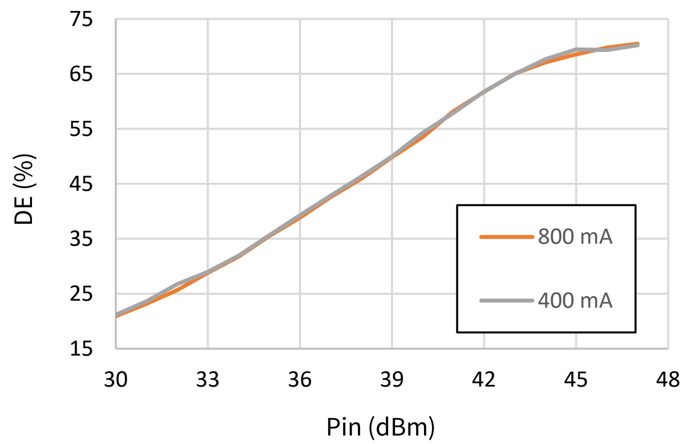


Figure 35: Id v. Pin v. Idq

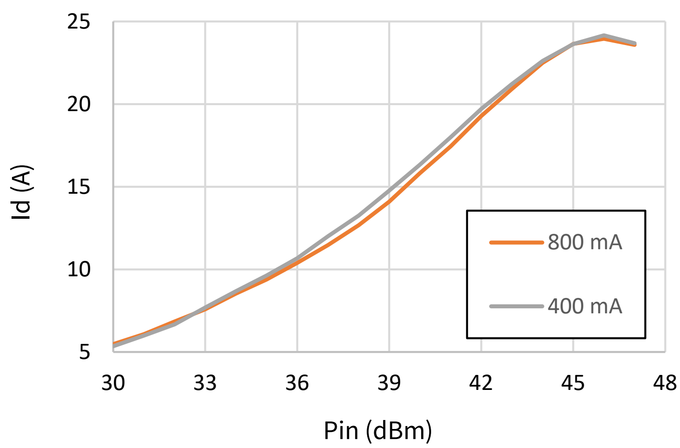


Figure 36: Ig v. Pin v. Idq

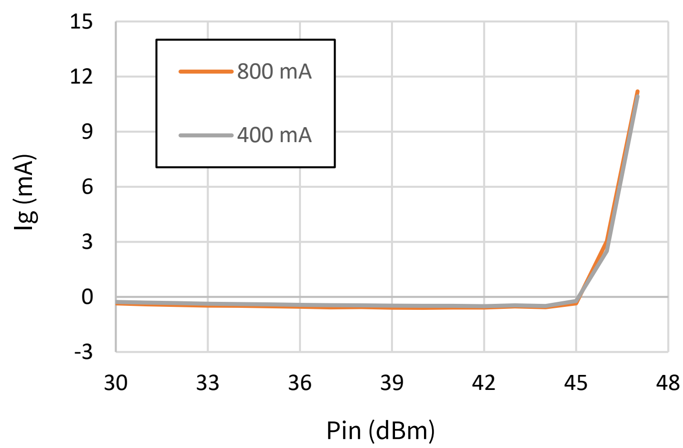
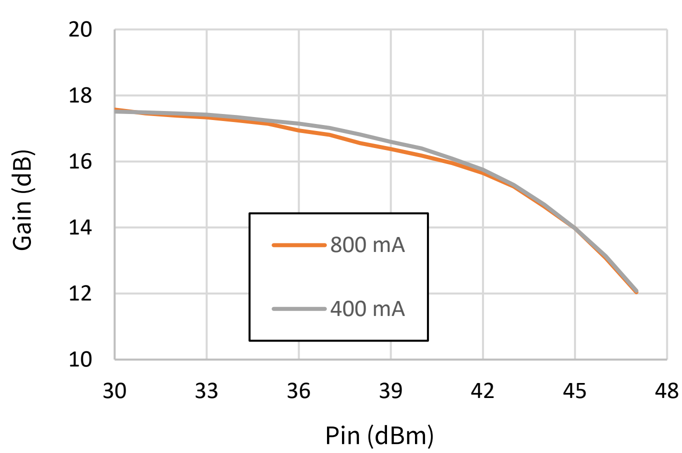


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, Pin = -20 dBm, T_{base}=25 °C

Figure 38: S21 v. Frequency v. Temperature

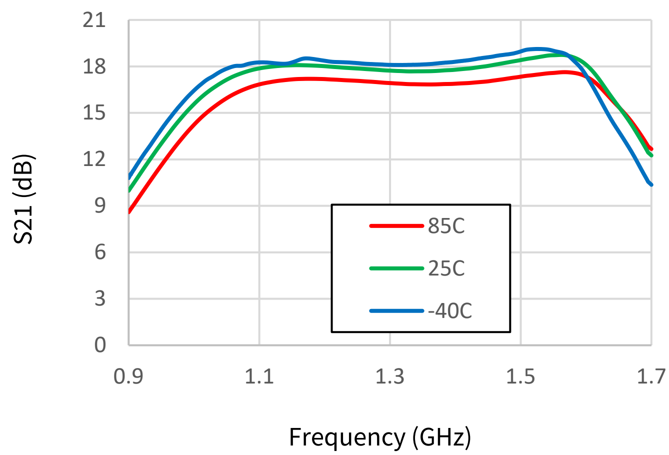


Figure 39: S21 v. Frequency v. Vd

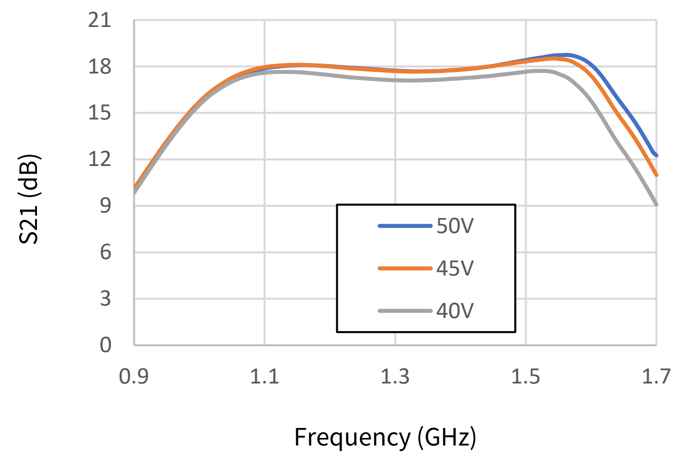


Figure 40: S11 v. Frequency v. Temperature

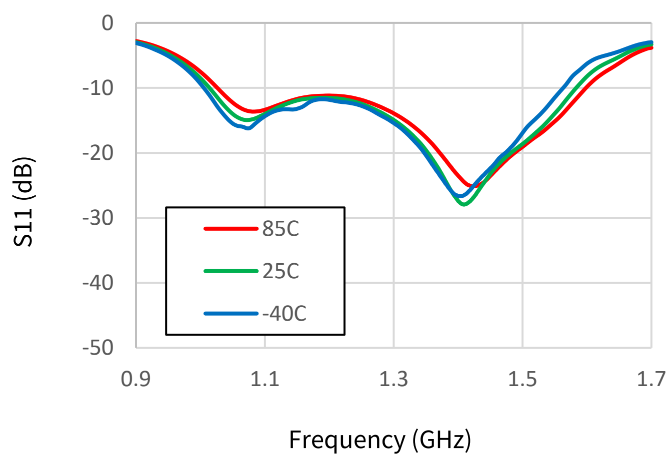


Figure 41: S11 v. Frequency v. Vd

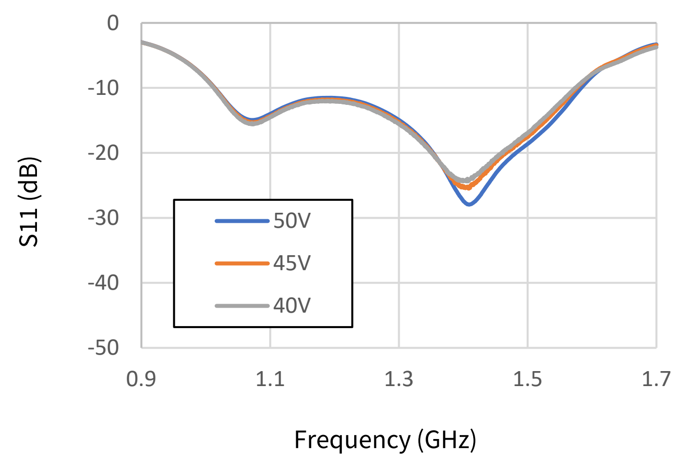


Figure 42: S22 v. Frequency v. Temperature

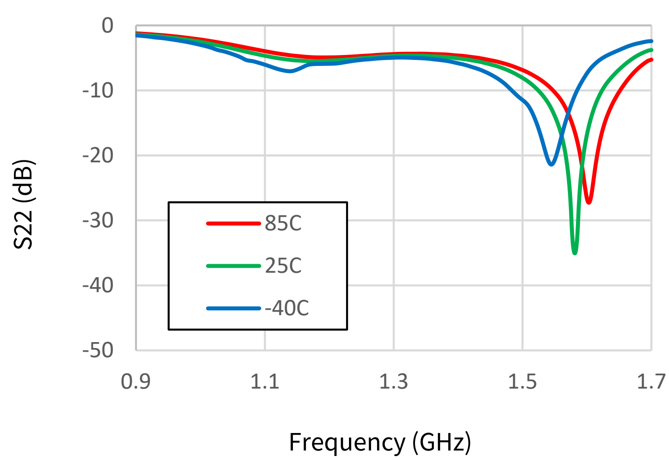
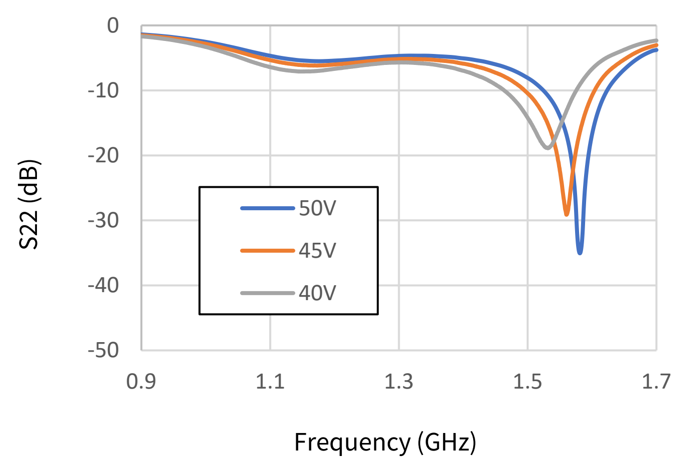


Figure 43: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, Pin = -20 dBm, T_{base}=25 °C

Figure 44: S21 v. Frequency v. Idq

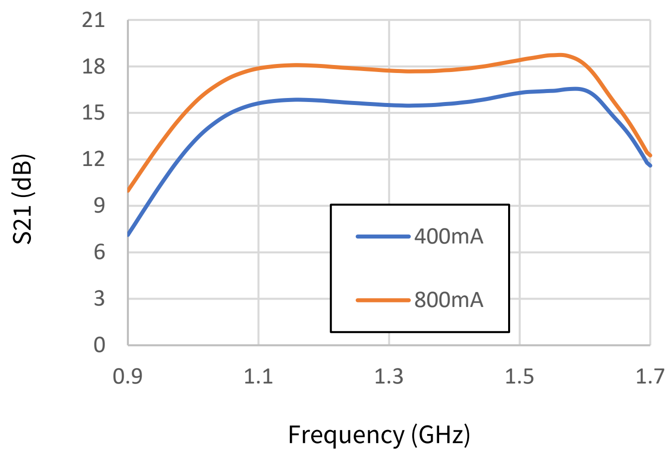


Figure 45: S11 v. Frequency v. Idq

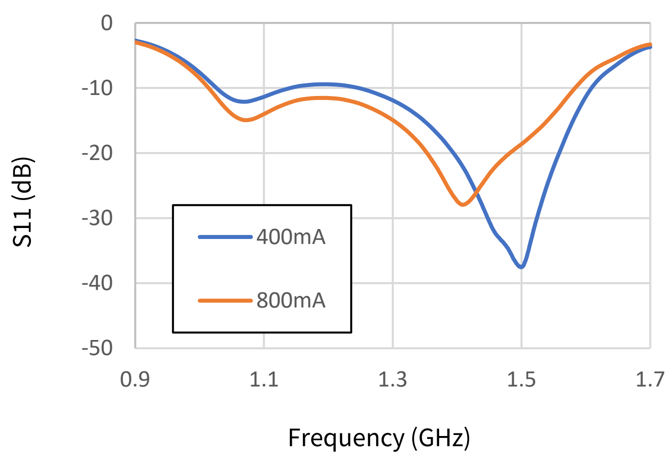
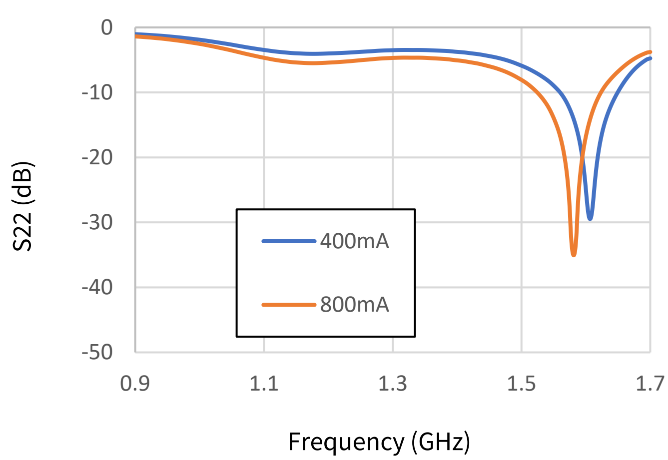


Figure 46: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=50V, Idq= 800mA, PW= 2ms, DC=20%, Pin = 45dBm, Frequency 1= 1.2 GHz, Frequency 2 = 1.3 GHz, Frequency 3 = 1.4 GHz, T_{base}=25 °C

Figure 53: f/2 v. Pout v. Temperature, F1

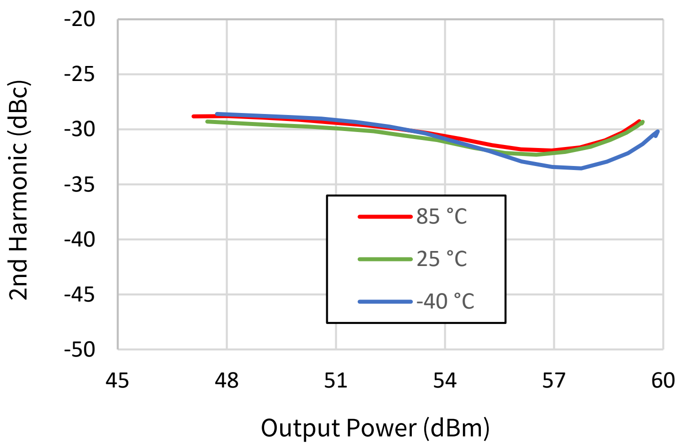


Figure 54: f/2 v. Pout v. Vd, F1

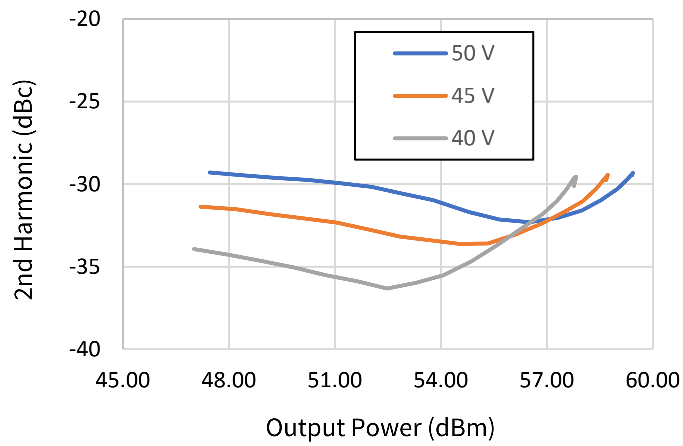


Figure 55: f/2 v. Pout v. Temperature, F2

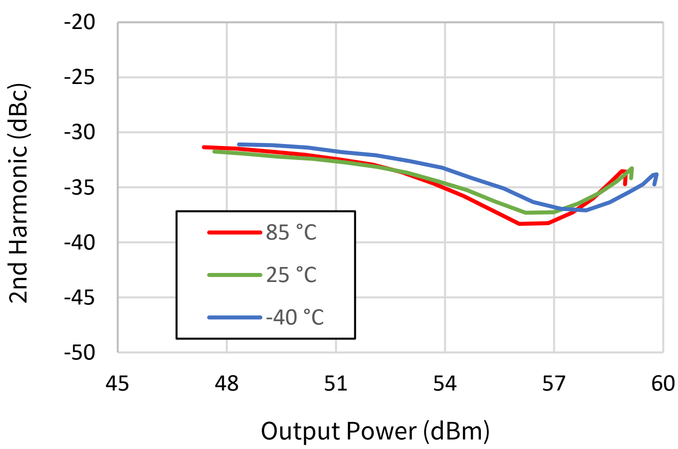


Figure 56: f/2 v. Pout v. Vd, F2

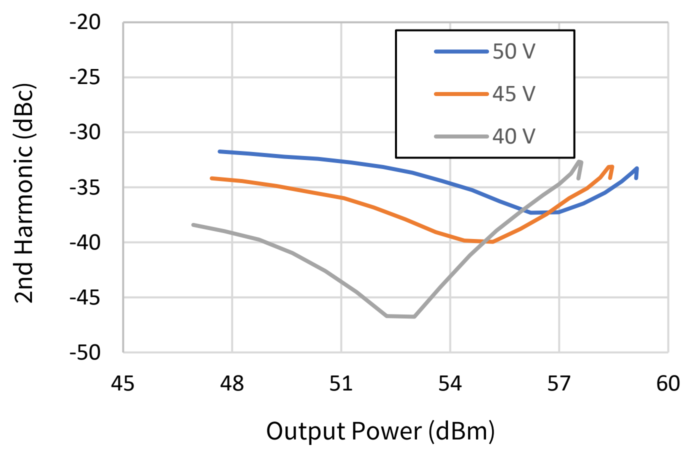


Figure 57: f/2 v. Pout v. Temperature, F3

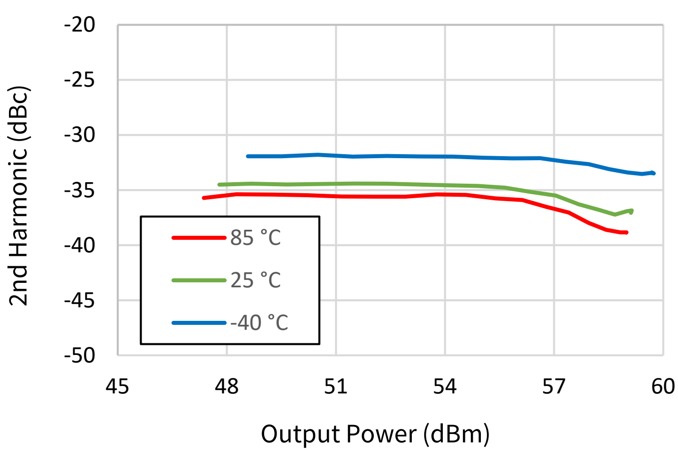
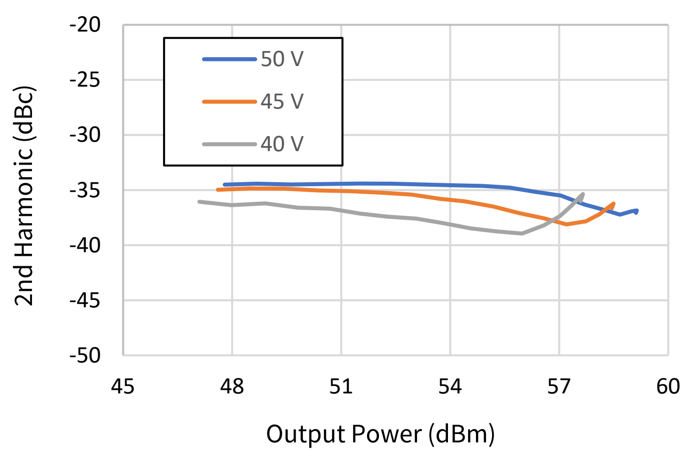


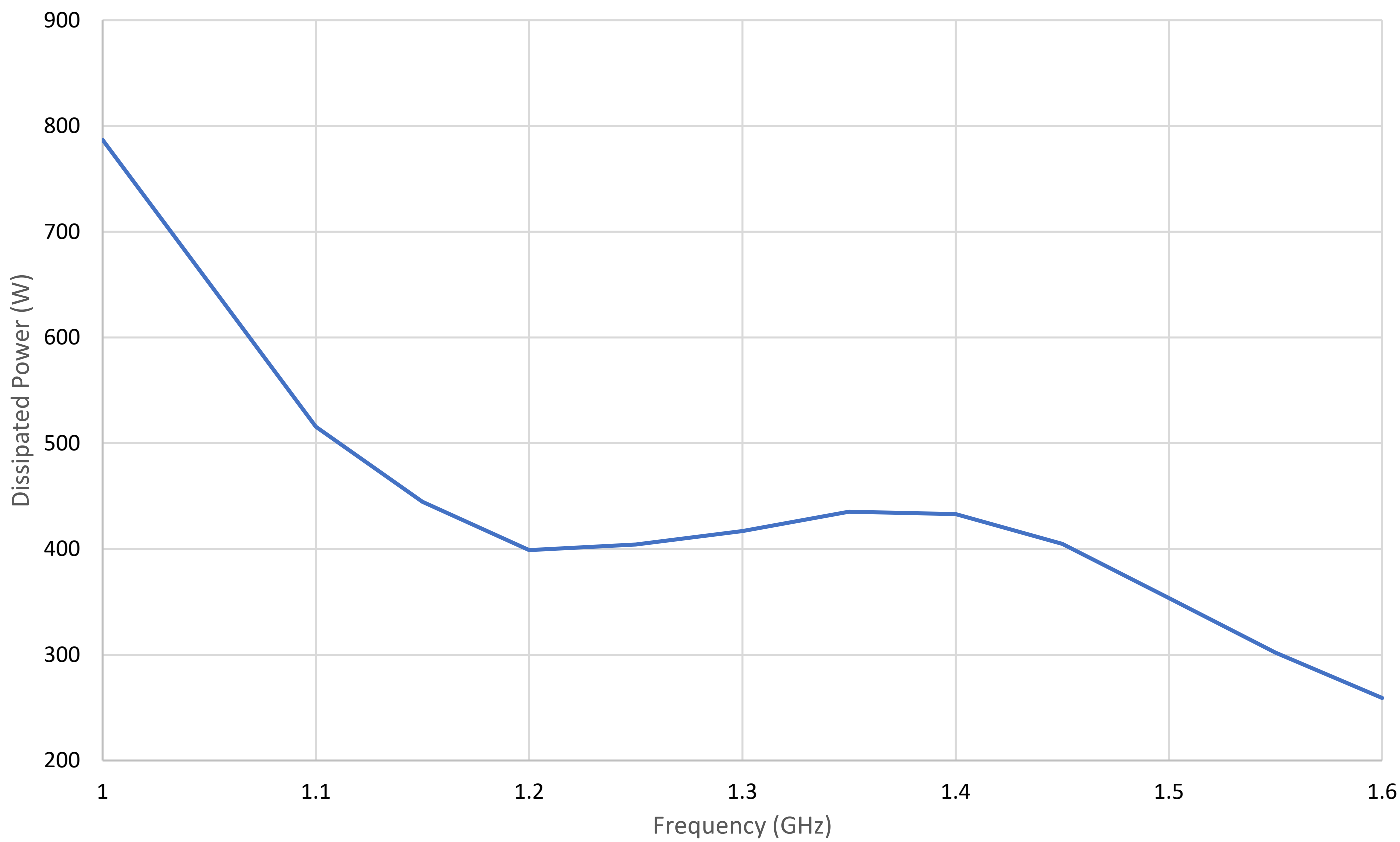
Figure 58: f/2 v. Pout v. Vd, F3



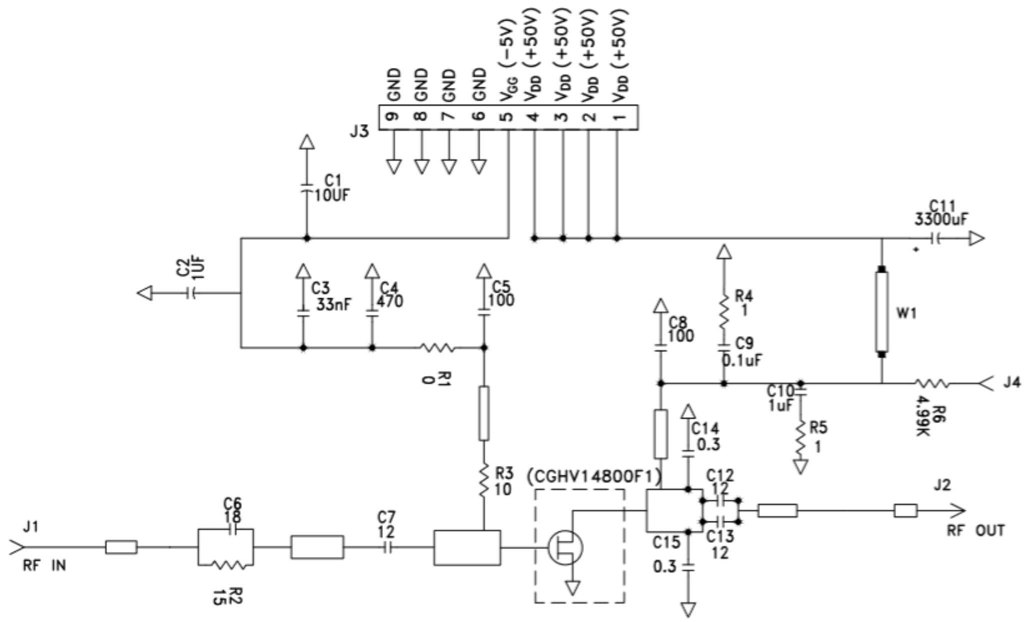
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	198	Freq = 1.4 GHz, V_d = 50 V, I_{dq} = 800 mA, I_{drive} = 23.0 A , P_{in} = 45 dBm, P_{out} = 58.6 dBm, P_{diss} = 433 W, T_{case} = 85°C, PW = 2ms, DC = 20%
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.26	

Power Dissipation v. Frequency (Tcase = 85°C)



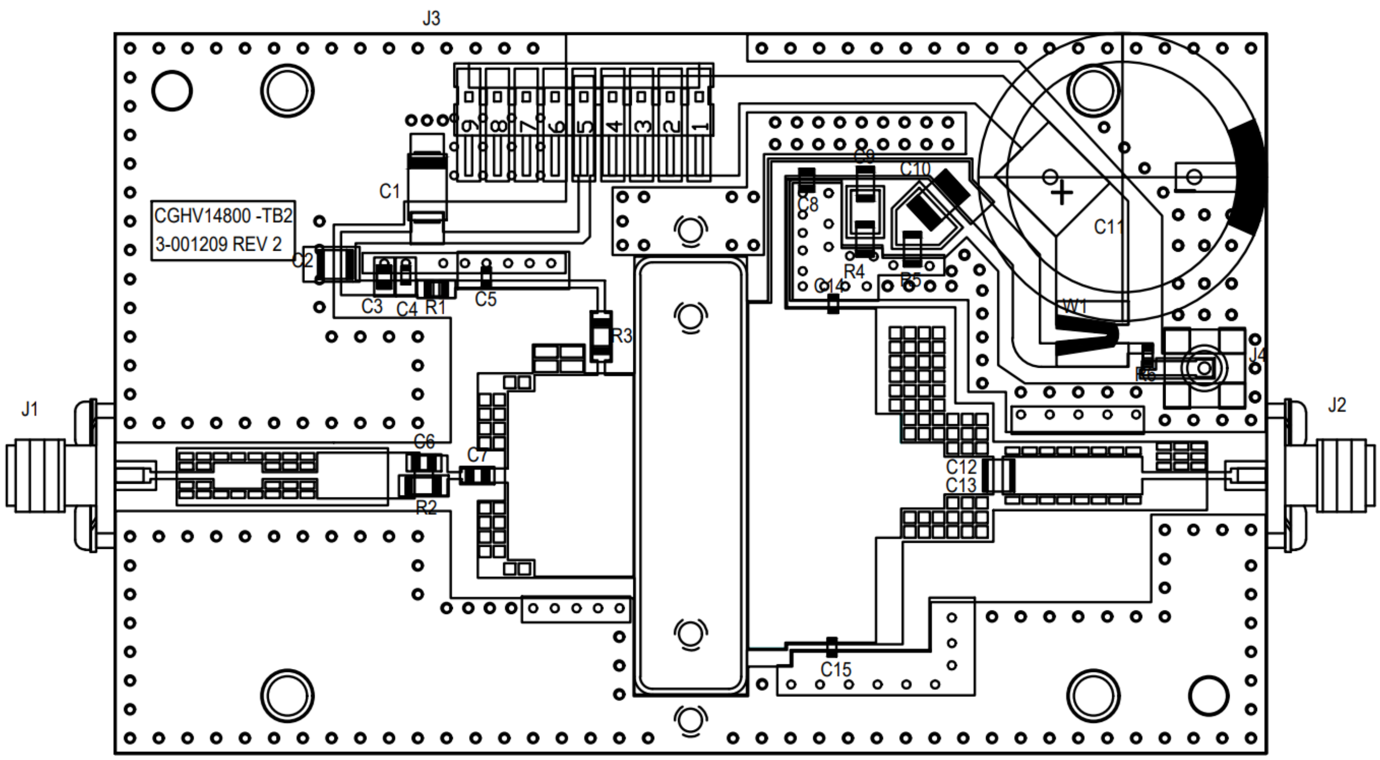
CGHV14800F1-AMP Evaluation Board Schematic Drawing



CGHV14800F1-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
R1	RES, 1/8W, 1206, 5%, 0 OHMS	1
R2	RES, 1/8W, 1206, 5%, 15 OHMS	1
R3	RES, 1/8W, 1206, 5%, 10 OHMS	1
R4,R5	RES, 1/8W, 1206, 5%, 1 OHMS	2
R6	RES,1/16W,0603,1%,4.99K OHMS	1
C1	CAP 10UF 16V TANTALUM	1
C2, C10	CAP, 1.0UF, 100V, 10%, X7R, 1210	2
C3	CAP,33000PF, 0805,100V, X7R	1
C4	CAP, 470pF, 0805, 100V, C0G	1
C5, C8	CAP, 100PF, +/-5%, 250V, 0805, ATC 600F	2
C6	CAP, 18pF, +/-5%, 250V, 0603, ATC 600S	1
C7	CAP, 12 PF, +/- 5%, 250V, 0805, ATC 600F	1
C9	CAP, 0.1uF, +/- 10%, 100V, 1206, 1206	1
C11	CAP, 3300 UF, +/-20%, 100V, ELECTROLYTIC	1
C12, C13	CAP, 12PF, +/- 2%,500V, ATC800B	2
C14, C15	CAP, 0.3PF, +/- 0.05pF, 0603, ATC	2
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
W1	CABLE ,18 AWG, 4.2”	1
	PCB, Rogers 3010, 0.025” THK, CGHV14800 1.2-1.4GHZ	1
	BASEPLATE, COPPER, 4.00 X 2.50 X 0.49, ALTERNATE HOLE PATTERN	1
	2-56 SOC HD SCREW 1/4 SS	4
	#2 SPLIT LOCKWASHER SS	4
	Indium Foil in channel (0.0002" thick)	

CGHV14800F1-AMP Evaluation Board Assembly Drawing



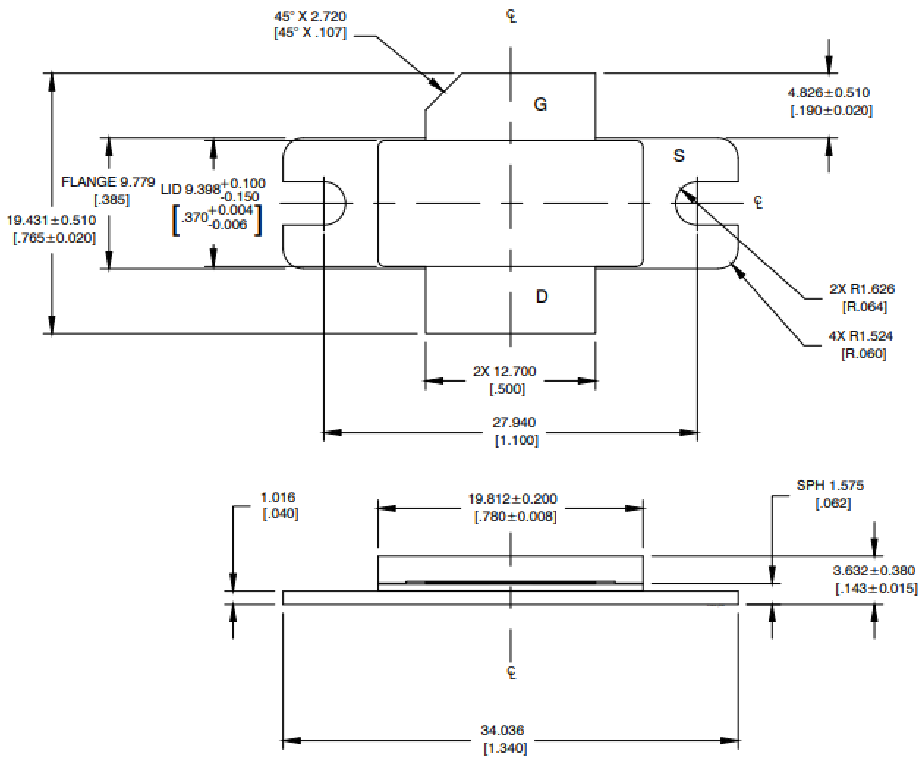
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

Bias Off Sequence

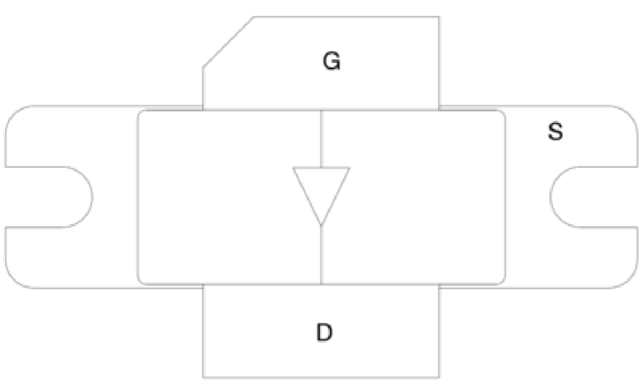
1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

Product Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. PINS: D=DRAIN
   S=SOURCE (FLANGE)
   G=GATE
3. LEAD THICKNESS: $0.10^{+0.051}_{-0.025}$ [$.004^{+.002}_{-.001}$]
4. PLATING (GOLD TOP LAYER): 1.14 ± 0.38 MICRON [45 ± 15 MICROINCH].
5. THE CONTENTS OF THIS DRAWING ARE INTENDED TO REPRESENT THE PRODUCT IN MARKETING GRAPHICS ONLY, AND NOT INTENDED TO BE USED FOR ANY PRODUCTION OR INTERNAL QUALIFICATION PURPOSE.



Pin	Description
D	Drain Device
G	Gate Device
S	Source (Flange)

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CGHV14800F1	DC – 1.4 GHz, 800W GaN Transistor	1 Each	
CGHV14800F1-AMP	1.2-1.4 GHz Evaluation Board	1 Each	

Notes & Disclaimer

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